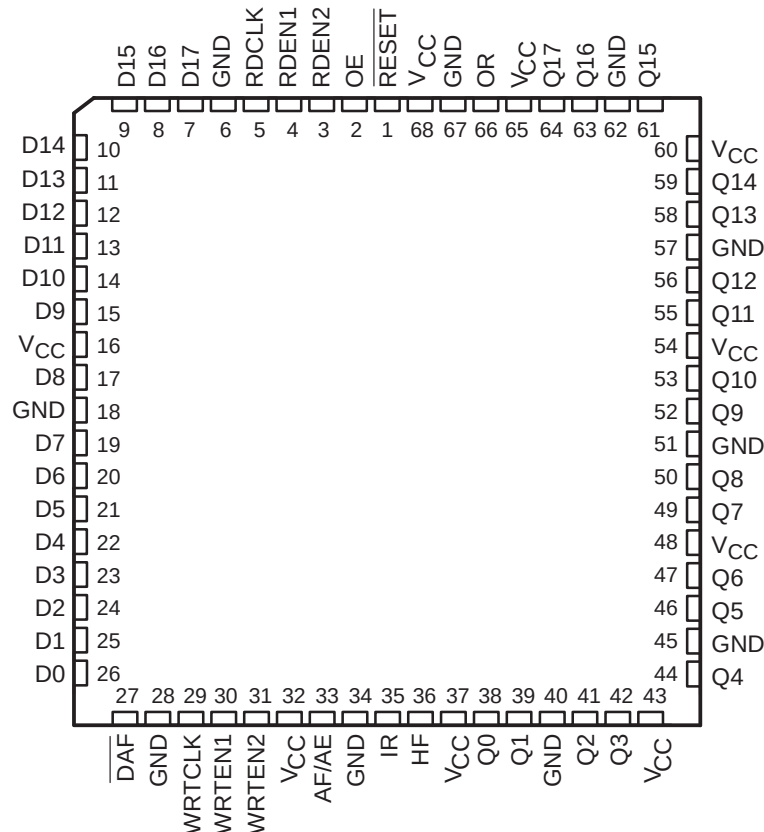


CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- 1024 Words × 18 Bits
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7884
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High-Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) and Space-Saving 80-Pin Thin Quad Flat (PN) Packages

FN PACKAGE
(TOP VIEW)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

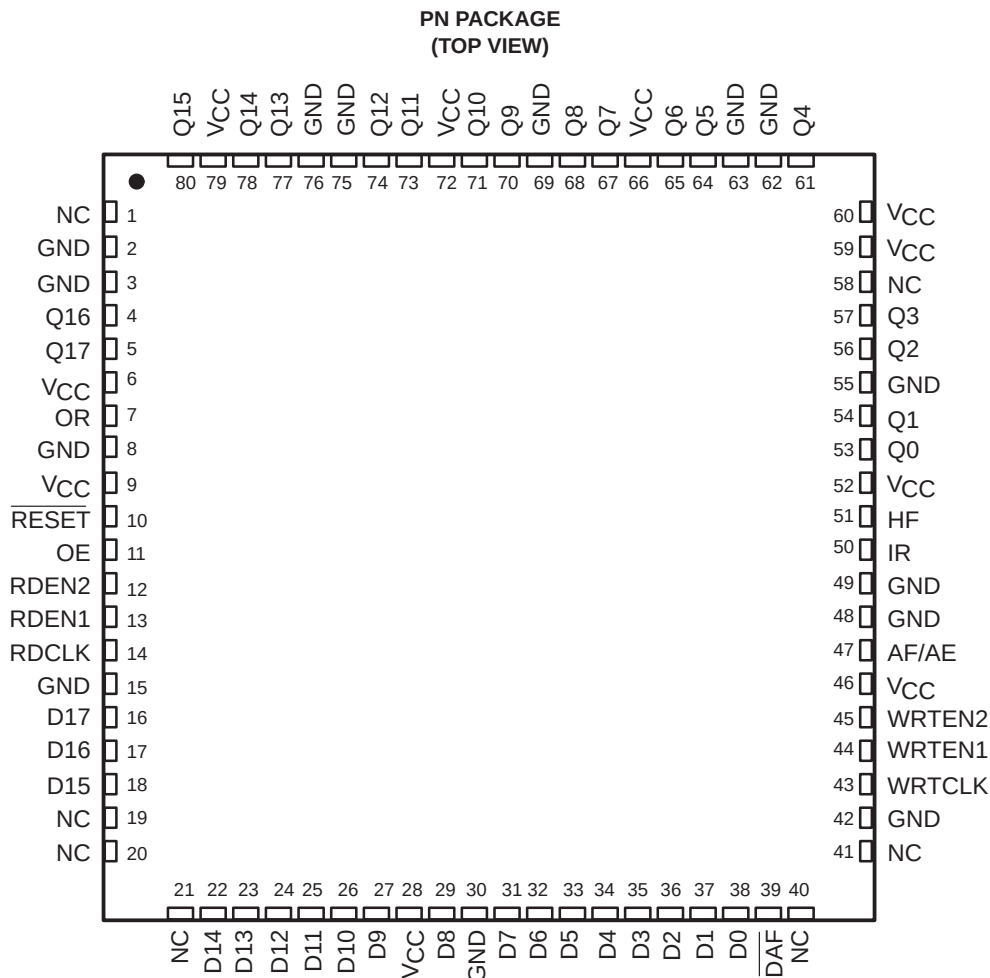
Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024 × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

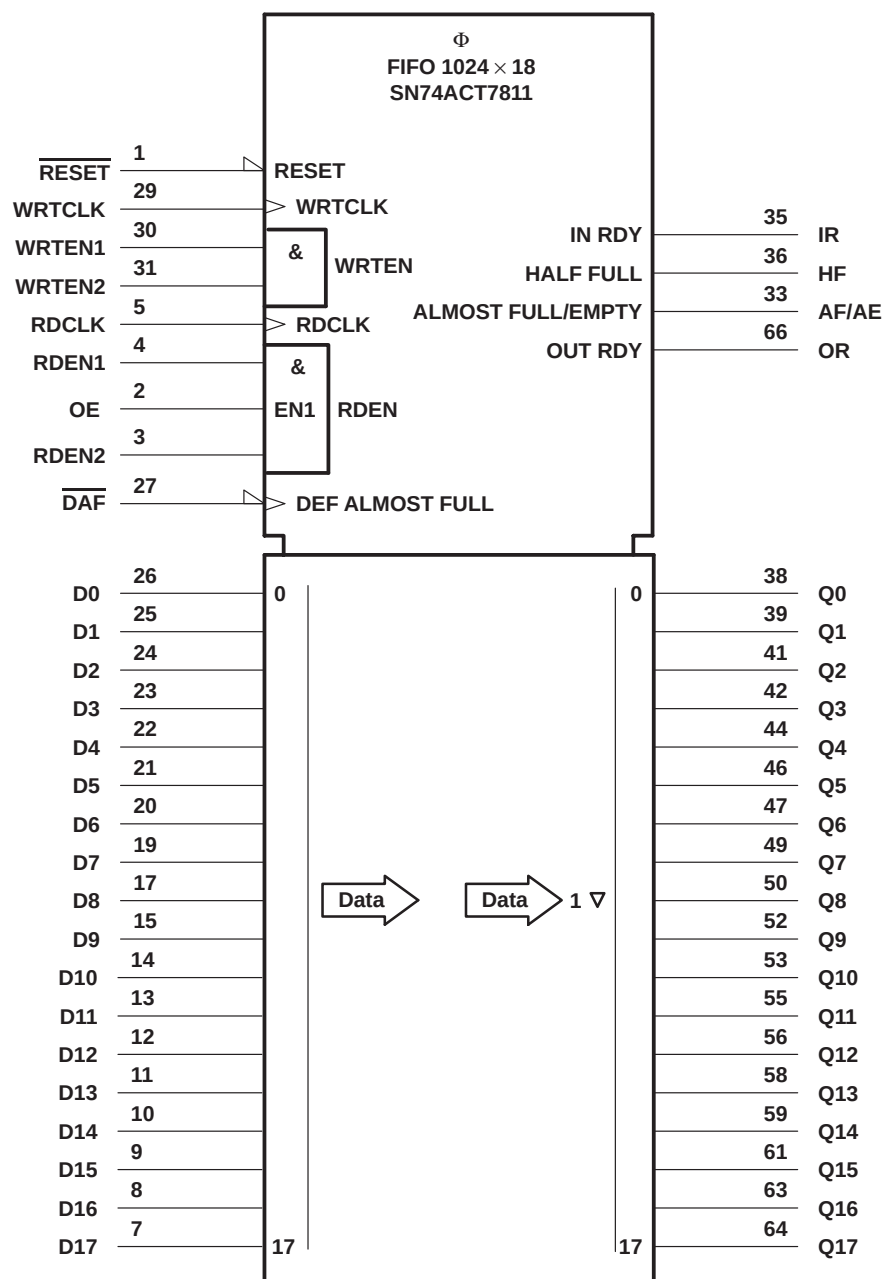
The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts or requests) to their respective system clock.

The SN74ACT7811 is characterized for operation from 0°C to 70°C.

CLOCKED FIRST-IN, FIRST-OUT MEMORY

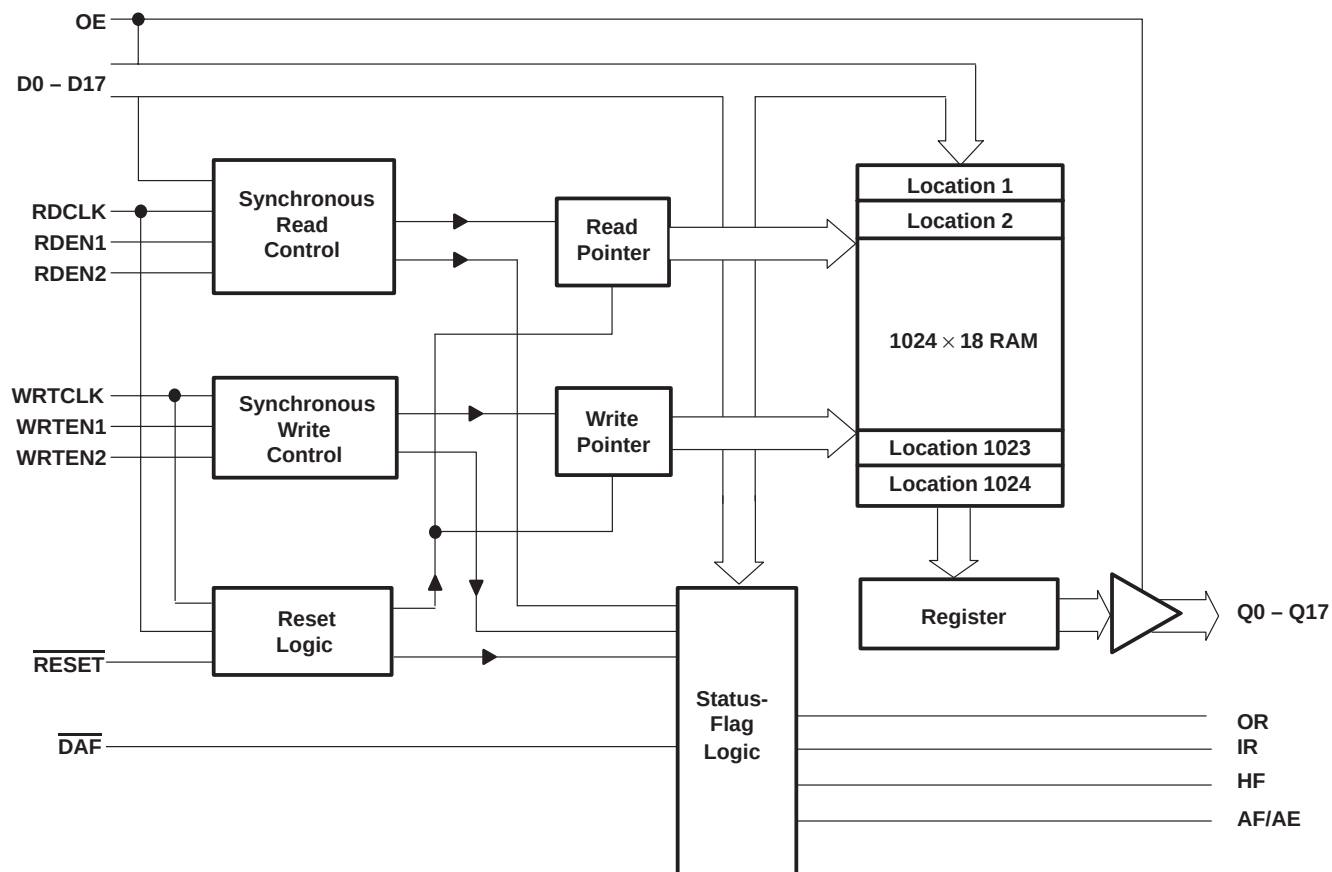
SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

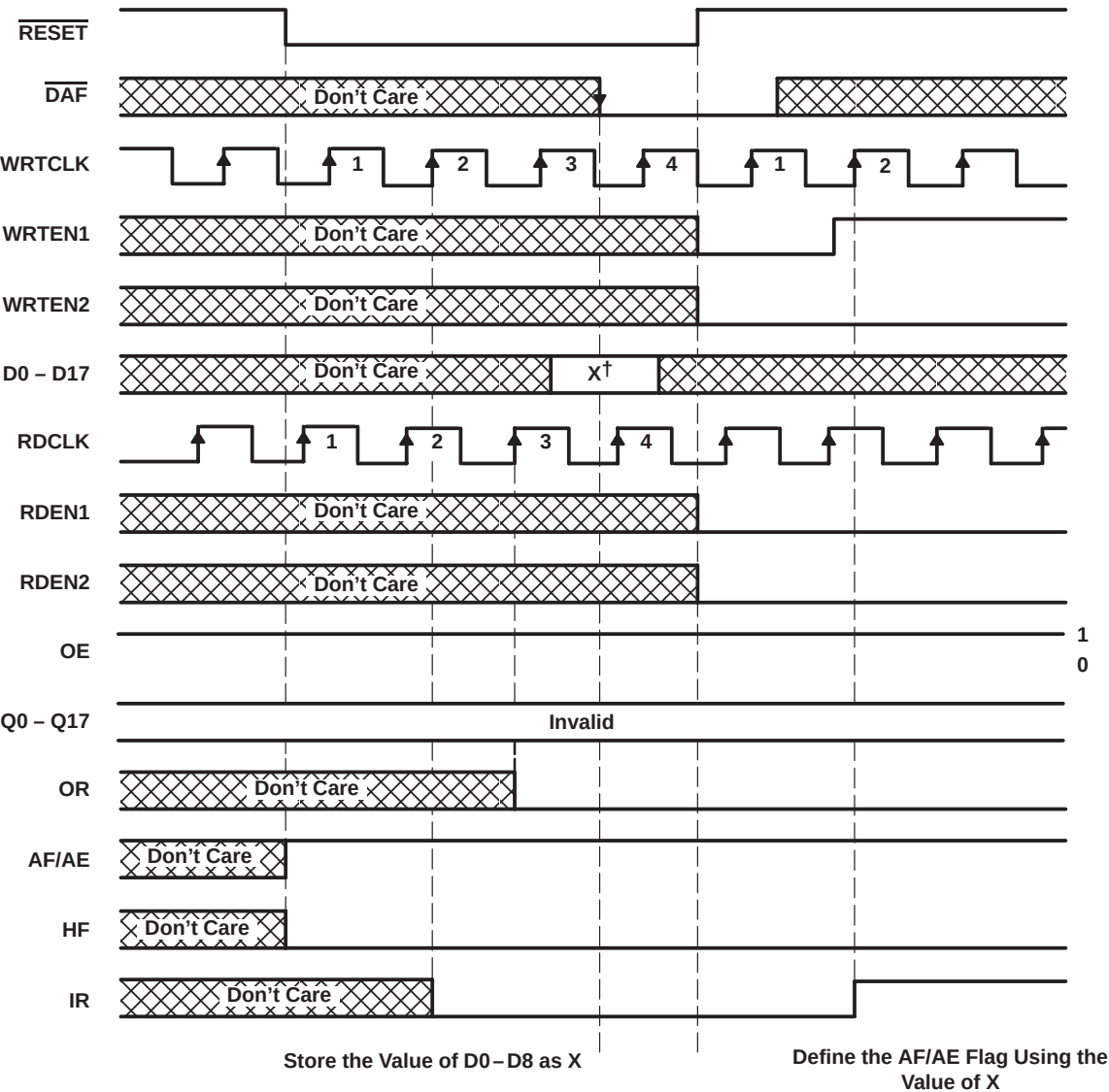
TERMINAL [†] NAME	NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or less words or (1025 - X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 - X) words. Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: <u>User-defined X</u> Step 1: Take $\overline{\text{DAF}}$ from high to low. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. <u>Default X</u> To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define almost full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0–D8 also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the $\overline{\text{DAF}}$.
HF	36	O	Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The data-out (Q0–Q17) outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and the OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE, and RDEN1 and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

[†] Terminals listed are for the FN package.

Terminal Functions (Continued)

TERMINAL [†] NAME	NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enables. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).

[†] Terminals listed are for the FN package.



[†] X is the binary value of D0-D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X

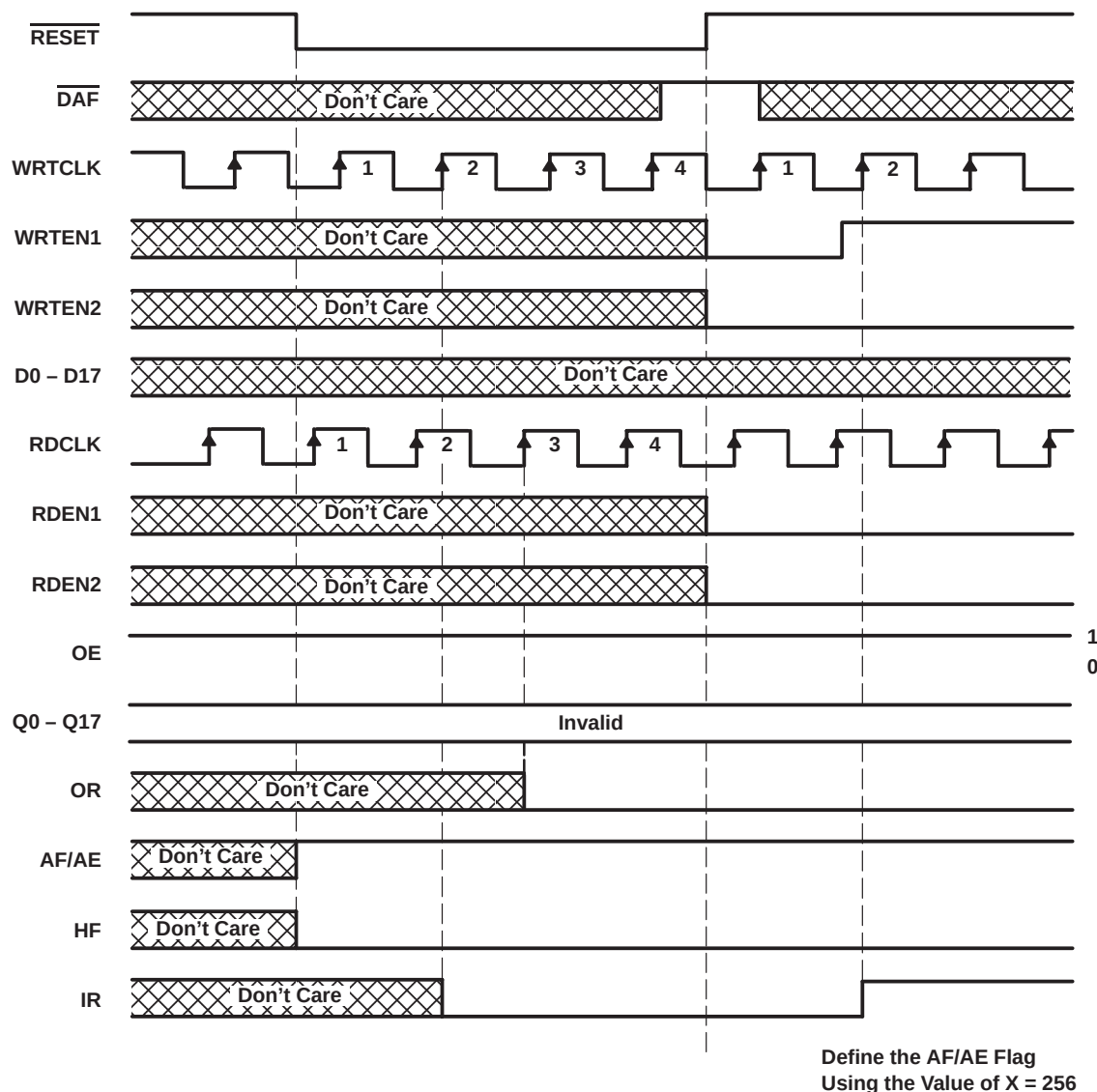


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

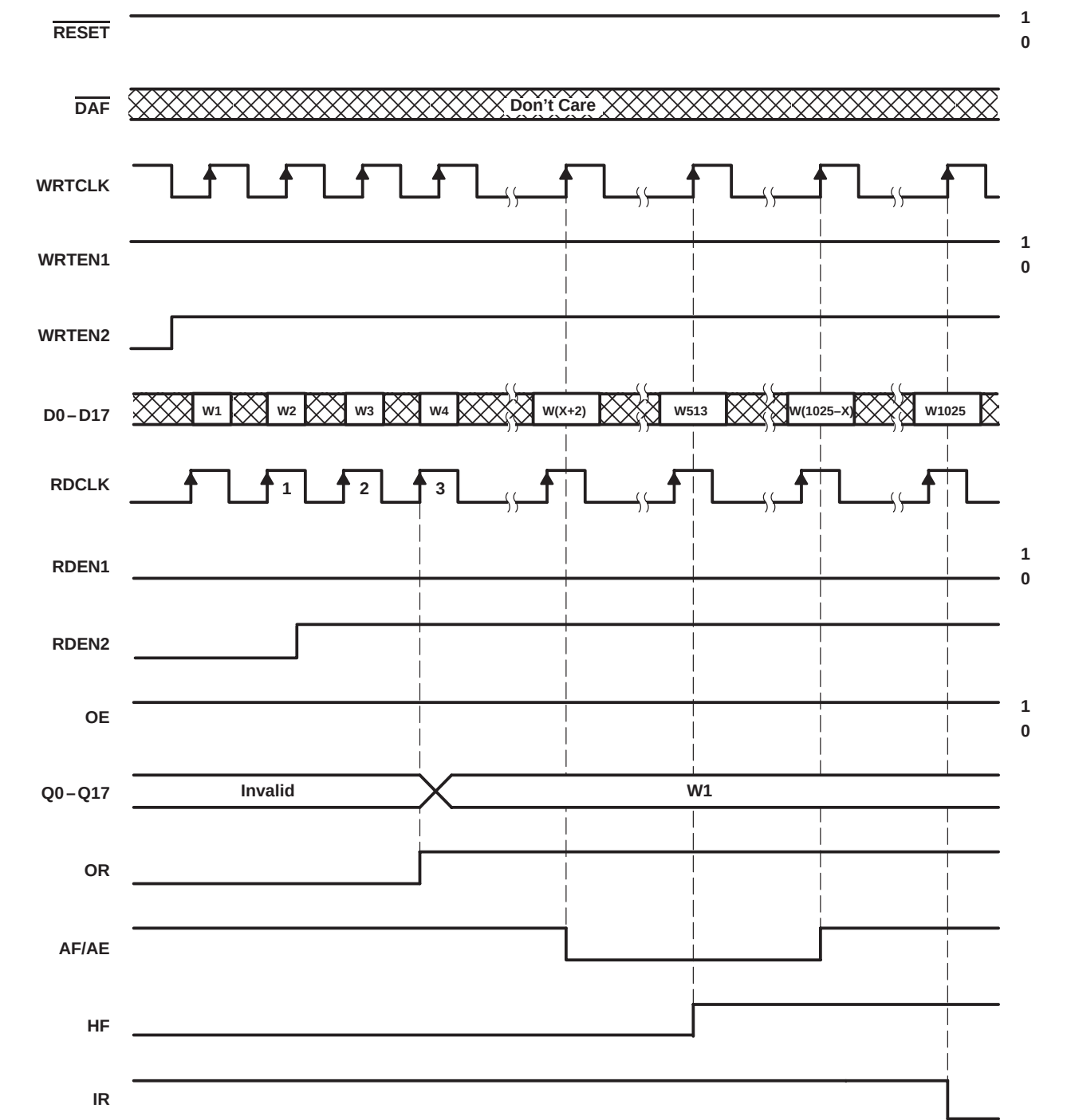


Figure 3. Write Cycle

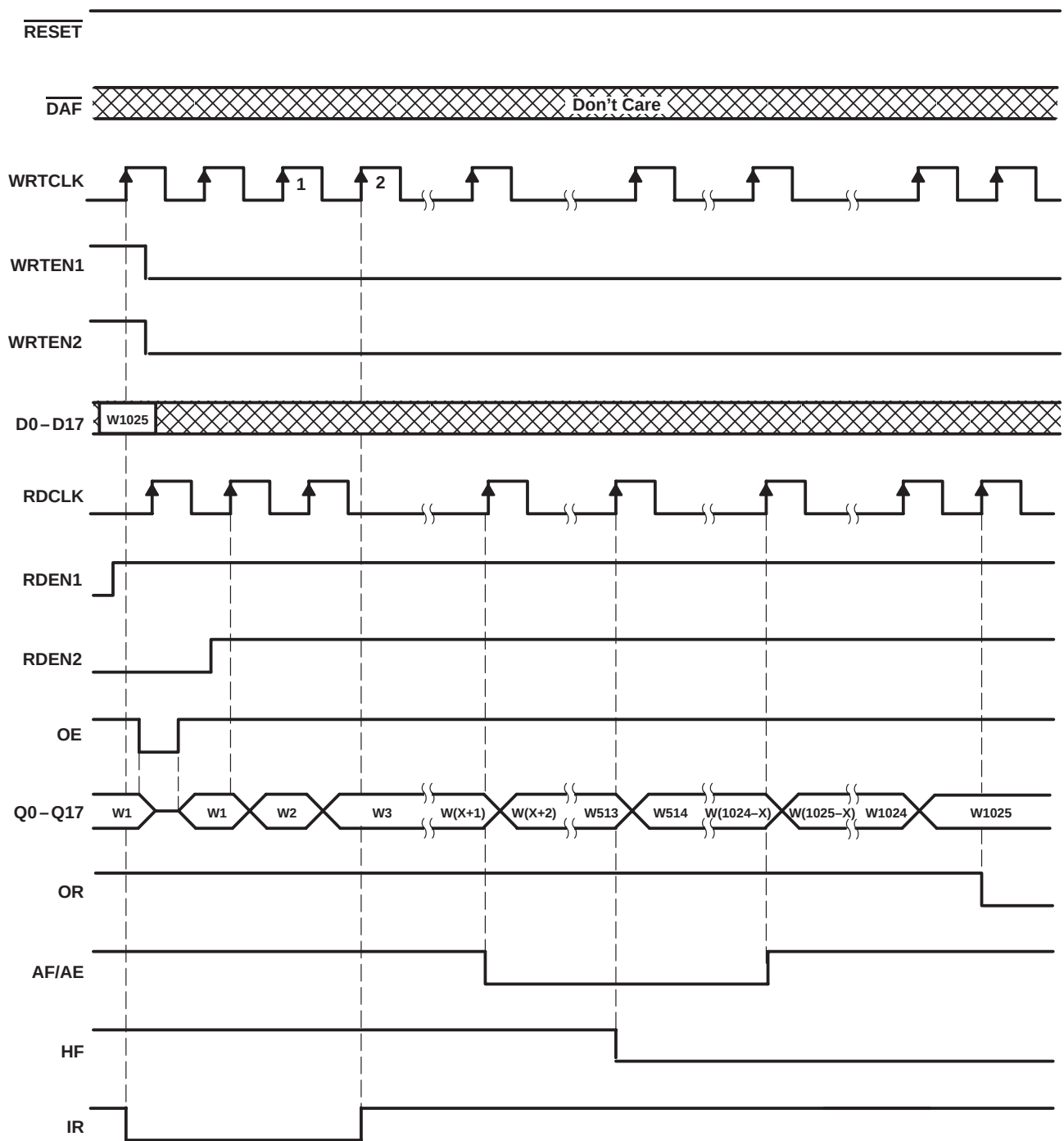


Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
I_{OH} High-level output current		–8	mA
I_{OL} Low-level output current		16	mA
T_A Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			V
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 16\text{ mA}$			0.5	V
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or 0 V			±5	μA
I_{OZ}	$V_{CC} = 5.5\text{ V}$, $V_O = V_{CC}$ or 0 V			±5	μA
$I_{CC}^{\S}$	$V_I = V_{CC} - 0.2\text{ V}$ or 0 V			400	μA
	One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i	$V_I = 0\text{ V}$, $f = 1\text{ MHz}$		4		pF
C_o	$V_O = 0\text{ V}$, $f = 1\text{ MHz}$		8		pF

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

^{\S} I_{CC} tested with outputs open

timing requirements (see Figures 1 through 8)

			'ACT7811-15		'ACT7811-18		'ACT7811-20		'ACT7811-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		40		35		28.5		16.7		MHz
t _w	Pulse duration	D0–D17 high or low	10		12		14		20		ns
		WRTCLK high	7		8.5		10		17		
		WRTCLK low	10		11		14		23		
		RDCLK high	7		8.5		10		17		
		RDCLK low	10		11		14		23		
		DAF high	10		10		10		10		
		WRTEN1, WRTEN2 high or low	10		10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		10		
t _{su}	Setup time	D0–D17 before WRTCLK↑	5		5		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	5		5		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	5		5		5		5		
		Reset: RESET low before first WRTCLK and RDCLK↑	7		7		7		7		
		Define AF/AE: D0–D8 before DAF↓	5		5		5		5		
		Define AF/AE: DAF↓ before RESET↑	7		7		7		7		
		Define AF/AE (default): DAF high before RESET↑	5		5		5		5		
t _h	Hold time	D0–D17 after WRTCLK↑	1		1		1		1		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	1		1		1		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	1		1		1		1		
		Reset: RESET low after fourth WRTCLK and RDCLK↑	0		0		0		0		
		Define AF/AE: D0–D8 after DAF↓	1		1		1		1		
		Define AF/AE: DAF low after RESET↑	0		0		0		0		
		Define AF/AE (default): DAF high after RESET↑	1		1		1		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 0°C to 70°C								UNIT	
			'ACT7811-15			'ACT7811-18		'ACT7811-20		'ACT7811-25		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN		MAX
f _{max}	WRTCLK or RDCLK		40			35		28.5		16.7		MHz
t _{pd}	RDCLK↑	Any Q	4	12	15	4	18	4	20	4	25	ns
t _{pd} [†]			10.5									
t _{pd}	WRTCLK↑	IR	2			10		2		14		ns
t _{pd}	RDCLK↑	OR	2			10		2		14		ns
t _{pd}	WRTCLK↑	AF/AE	6			20		6		24		ns
	RDCLK↑		6			20		6		24		
t _{PLH}	WRTCLK↑	HF	6			19		6		23		ns
t _{PHL}	RDCLK↑		6			19		6		23		
t _{PLH}	RESET↓	AF/AE	3			19		3		23		ns
t _{PHL}		HF	4			21		4		25		
t _{en}	OE	Any Q	2			11		2		11		ns
t _{dis}			2			14		2		14		

[†] This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per 1K bits	C _L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

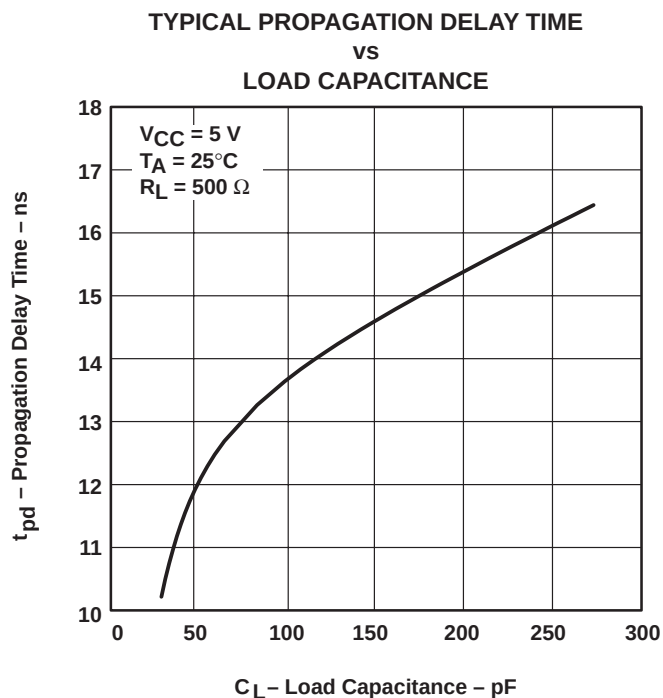


Figure 5

TYPICAL CHARACTERISTICS

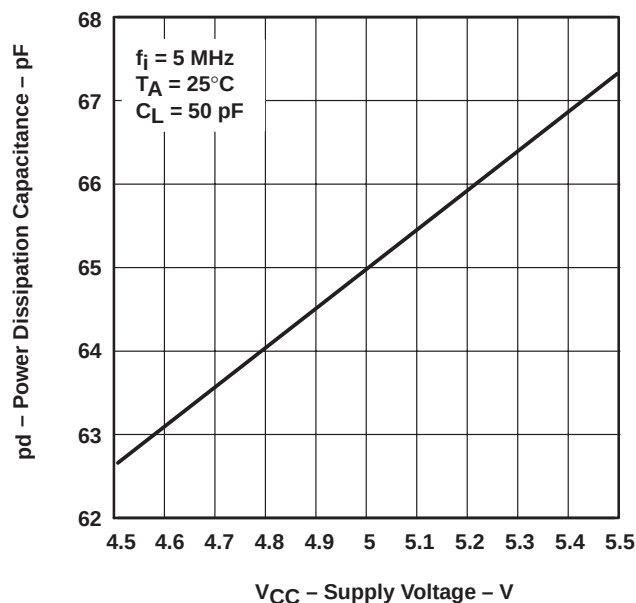
TYPICAL POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7811 can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

- I_{CC} = power-down I_{CC} maximum
- N = number of inputs driven by a TTL device
- ΔI_{CC} = increase in supply current
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_{pd} = power dissipation capacitance
- C_L = output capacitive load
- f_i = data input frequency
- f_o = data output frequency

APPLICATION INFORMATION

expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

After the first data word is loaded into the FIFO, the word is unloaded and the output-ready flag (OR) output goes high after $(N \times 3)$ read-clock (RDCLK) cycles, where N is the number of devices used in depth expansion.

After the FIFO is filled, the input-ready flag (IR) output goes low, the first word is unloaded, and the IR flag output is driven high after $(N \times 2)$ write-clock cycles, where N is the number of devices used in depth expansion.

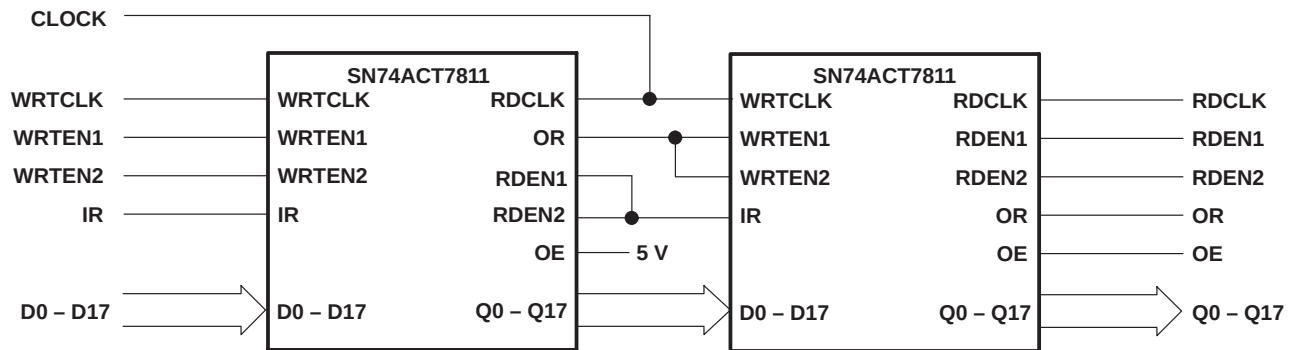


Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, $N = 2$

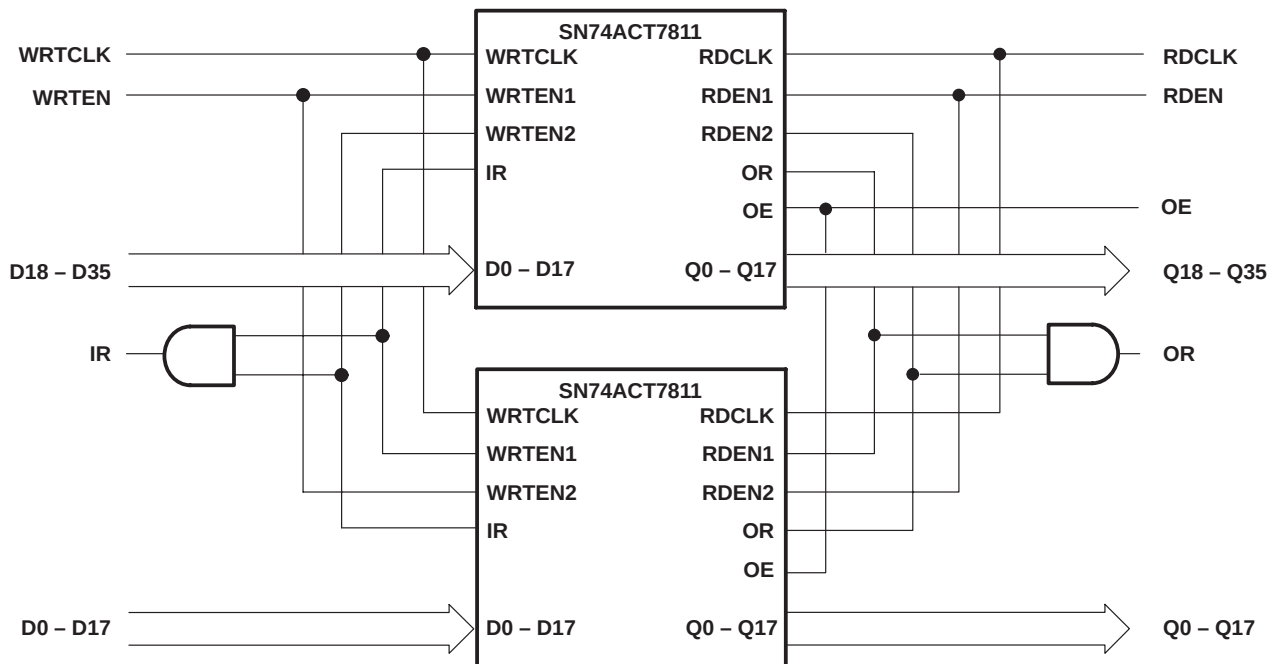
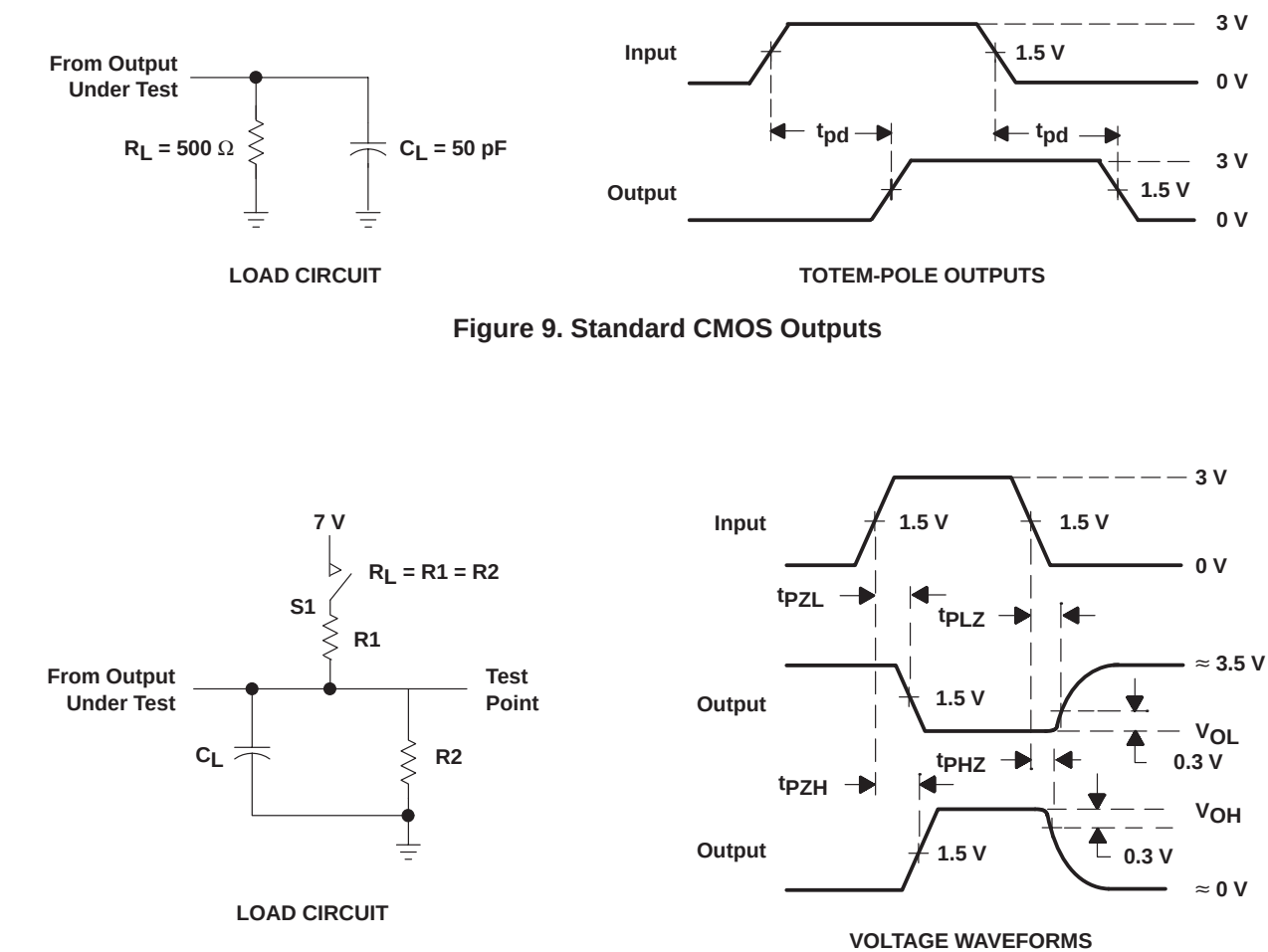


Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

PARAMETER MEASUREMENT INFORMATION



PARAMETER		R1, R2	$C_L^\dagger$	S1
t_{en}	t_{pZH}	500 Ω	50 pF	Open
	t_{pZL}			Closed
t_{dis}	t_{pHZ}	500 Ω	50 pF	Open
	t_{pLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs (Any Q)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ACT7811-15FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-15PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-18FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-18FNR	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-18PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-20FN	NRND	PLCC	FN	68	18	TBD	Call TI	Call TI
SN74ACT7811-20PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-25FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-25PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

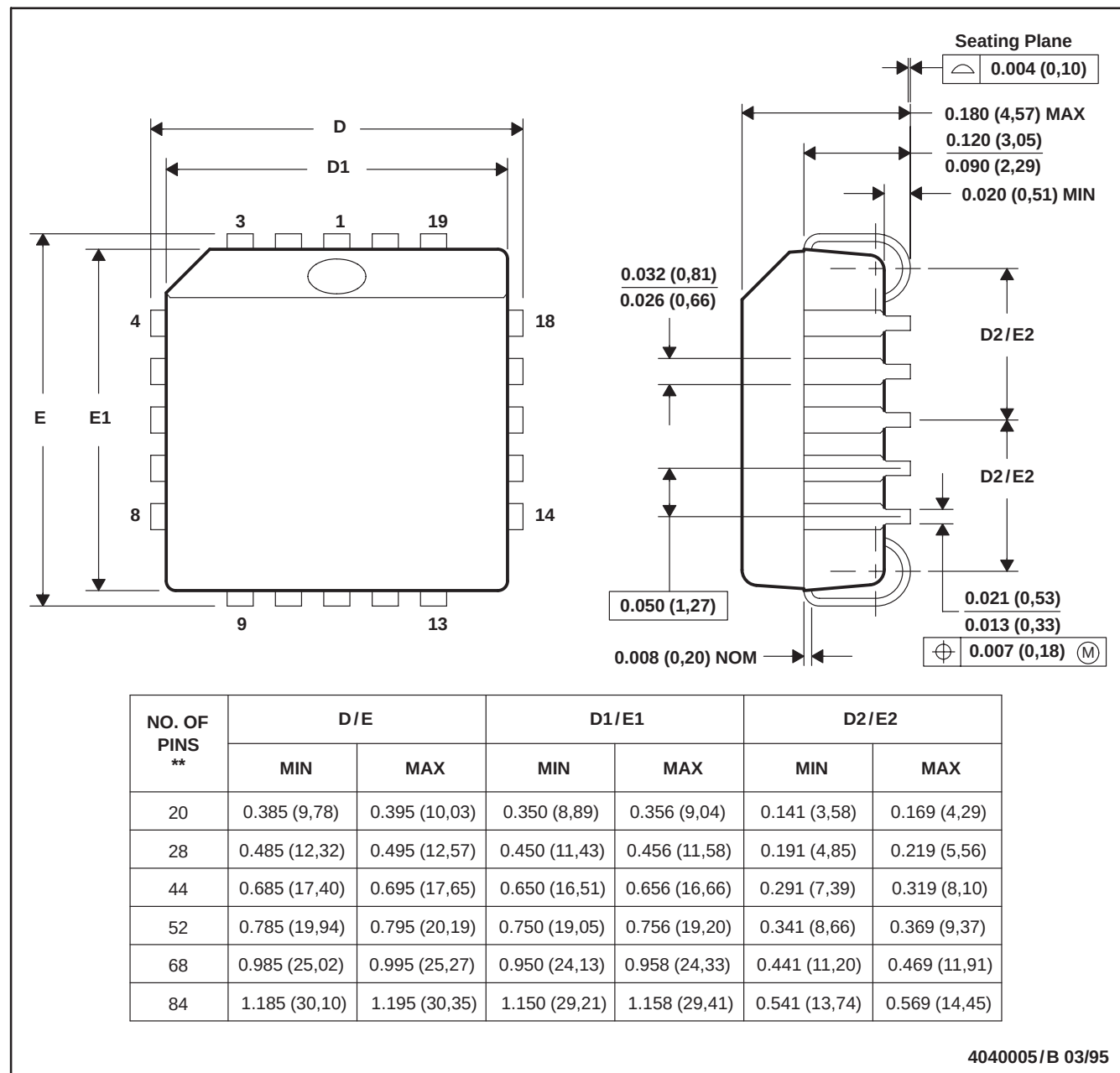
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

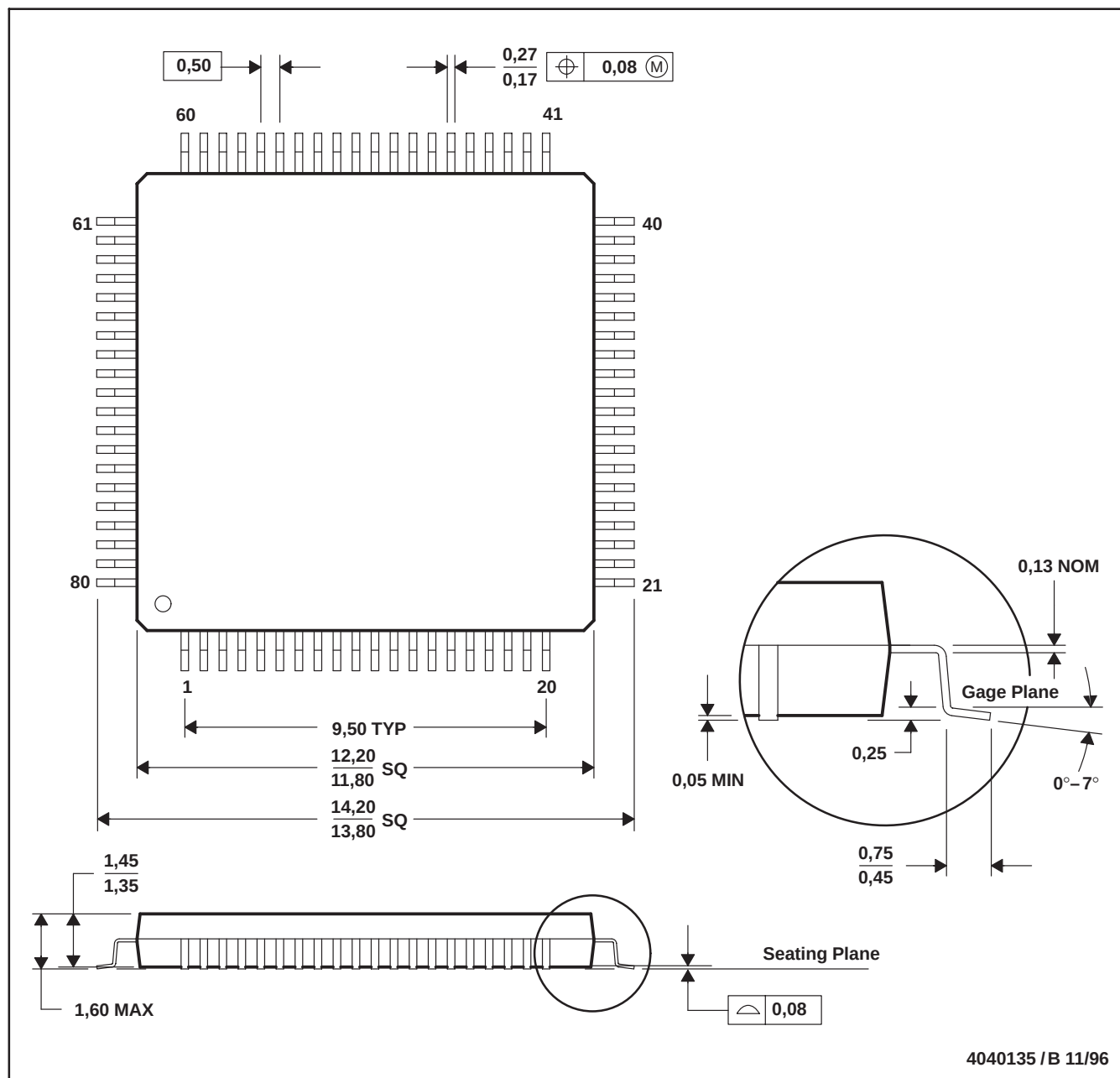
20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

PN (S-PQFP-G80)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
Low Power Wireless	www.ti.com/lpw

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated